Roll No. | | | | | | | | | | |

Total No. of Questions : 09 Total No. of Pages : 02

B.Tech. (AI & ML/ AI & DS/CSE/Cyber Security/DS/IOT and Cyber Security including Block chain Technology) (Sem.–4)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTES-401-18

M.Code : 77627

Date of Examination : 06-06-2025

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION - A

1. **Write briefly :**

   a) CPU

   b) Memory transfer instruction

   c) Control Unit

   d) Three address instruction

   e) DMA

   f) Cache memory

   g) SCII

   h) USB

   i) I's complement

   j) Carry look ahead adder

SECTION - B

2. Explain any 5 addressing modes with example.

3. Discuss the various representations of positive and negative number. Which representation is used by computer and why?

4. Differentiate between synchronous and asynchronous data transfer.

5. What is virtual memory? What is the concept of page replacement?

6. Write a note on cache coherency and concurrent access to memory.

SECTION - C

7. Explain how addition and subtraction takes place in computer system.

8. Differentiate between privileged and non-privileged instructions, hardware and software interrupts.

9. Describe memory hierarchy and memory interleaving in detail.

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Total No. of Questions : 09

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B.Tech. (AI & ML / AI & DS / CSE / Internet of Things and Cyber Security including Block Chain Technology) (Sem.–4)

COMPUTER ORGANIZATION & ARCHITECTURE

Subject Code : BTES 401/18

M.Code : 77627

Date of Examination : 14-12-2024

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
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3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Write briefly :**

   a. Cache Memory

   b. Register Transfer Language

   c. Normalization of Floating Point Representation

   d. Accumulator

   e. Subroutine

   f. Instruction Format

   g. Clock pulse

   h. Hardwired Control

   i. Purpose of Interrupt signal.

   j. Speedup in Pipeline.

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SECTION-B

2. Explain in detail Instruction Set architecture of a CPU.
3. Explain in detail Purpose and Types of Interrupts.
4. List Benefits and Hazards of using Pipeline.
5. What do you understand by Memory interleaving? Explain in detail.
6. Explain in detail the working of Floating Point Arithmetic by suitable examples.

SECTION-C

7. Briefly explain the block diagram and instruction set of 8085 processor.
8. Explain in detail how I/O transfers is performed in x86 architecture.
9. Explain in detail the role performed by Mapping functions and Replacement Algorithms in memory.

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B.Tech. (AI & ML/CSE/DS/IT/ Internet of things and Cyber Security including Blockchain Technology) (Sem.–4)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTES-401-18

M.Code : 77627

Date of Examination : 23-05-2024

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Write briefly :**

   a) Write functioning of USB?

   b) What do you mean by floating point arithmetic?

   c) What is difference between SPMD and MIMD machine?

   d) What do you mean by I/O processors?

   e) Differentiate between program interrupt and subroutine call.

   f) What is meant by Interleaved memory?

   g) Write down two properties of SIMD.

   h) Distinguish between Isolated and Memory-Mapped I/O.

   i) Distinguish between static RAM and dynamic RAM.

   j) Name various interrupts in 8085.

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SECTION-B

2. Show a step-by-step multiplication process using Booth's algorithm to multiply two numbers 17 * (-7).

3. Explain what different types of memories are available and differentiate between them according to their application?

4. Discuss the fetch-decode and execute cycles of a processor.

5. Write the basic feature of static and dynamic memory. Also give an example.

6. Discuss the role of cache coherency in parallel processors.

SECTION-C

7. Explain in detail the different mappings used for cache memory. Compare them.

8. With a neat block diagram, explain how the DMA controller is initialized for DMA data transfer?

9. Write short notes on the following :

   a) SMIMD

   b) Pipelining in CPU design.

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B.Tech. (AI&ML/AI & Data Science/CE/CSE) (Sem.–4)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTES-401-18

M.Code : 77627

Date of Examination : 05-12-2023

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

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3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Write briefly :**

   a) What is I/O subsystem?

   b) Discuss ripple carry adder.

   c) What is hardwired design?

   d) Write functioning of SCII.

   e) What is meant by non restoration?

   f) Write use of DMA.

   g) What are privileged instructions?

   h) Discuss mapping function.

   i) Briefly explain block size.

   j) What are pipeline hazards?

SECTION-B

2. Briefly explain computer instructions formats and sets.

3. What do you understand by interrupt? Explain the steps through which the processor handles the interrupts.

4. What are the benefits of hardwired and microprogrammed design approaches?

5. Discuss the use of cache coherency in parallel processors.

6. How floating point representation and character representation is done in computer organization?

SECTION-C

7. Briefly explain the block diagram and instruction set of 8085 processor? How 8085 is different from 8086?

8. What is the concept of hierarchical memory organization? Discuss its benefits in computer organization.

9. Discuss the basic concept of Pipelining in data processing. How it is used in speedup?

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B.Tech. (Artificial Intelligence & Machine Learning/Computer Engineering/Computer Science & Engineering/Computer Science & Engineering (Artificial Intelligence & Machine Learning)/ Information Technology/CSE (Internet of Things and Cyber Security including Block Chain Technology)/ CSE (PIT)) (Sem.–4)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTES-401-18

M.Code : 77627

Date of Examination : 05-07-22

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

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3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Write briefly :**

   a) What is Control Unit?

   b) Discusss carry look-ahead adder.

   c) Write functioning of USB.

   d) Define concept of Memory Organization.

   e) What is meant by division restoration?

   f) Write use of software interrupts?

   g) What are CPU registers?

   h) Discuss floating point arithmetic.

   i) Briefly explain cache size?

   j) List advantages of pipelining?

SECTION-B

2. Explain different addressing modes used in central processing unit.

3. What are the advantages and disadvantages of hardwired and microprogrammed design approaches?

4. What is DMA? Give an example, where DMA mode of data transfer is useful.

5. Discuss the role of cache coherency in parallel processors?

6. How the data is represented in computer architecture? Explain with example

SECTION-C

7 Briefly explain the block diagram and instruction set of 8085 processor? How 8085 is different from 8086?

8. What is the need of replacement algorithms in memory organization? Explain with example.

9. Discuss the role of pipelining for data processing in computer organization. How it increases the throughput?

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